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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/602,901	PETERSON ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *1,8,14,19,26 and 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-7,9-13,15-18,20-25,27-30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed August 3, 2004 with respect to the rejections of claims 2-7, 9-13, 15-18, 20-25, 27-30, and 32-39 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Ottinger (U.S. Patent No. 6,070,231) and Chin et al. (U.S. Patent No. 6,160,562).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-7, 9-13, 15-18, 32-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox (U.S. Patent No. 5,357,621) in view of Ottinger (U.S. Patent No. 6,070,231).

Referring to claims 4, 10, 16, 35, and 37, Cox teaches a memory system network consists of a central memory system controller and at least one individually addressable memory module controller coupled serially to the memory system controller. Various command signals generated by the memory system controller and information or data signals generated either by the memory system controller or individual memory module controllers in response to commands transmitted from the system controller, are transmitted and received serially between the system controller and the memory module controllers (col. 2, lines 36-50). The expandable memory system utilizes a plurality of plug-in, add-on memory modules or memory cards wherein each individual

memory module comprises a module controller, a module memory address control logic block and at least one memory block having a number of individually addressable memory cells (memory sub-array) (col. 2, lines 53-59, also with reference to Fig. 1). Cox also teach the system includes the capability to bypass or disable bad memory modules and reassign memory addresses without leaving useable memory unallocated (col. 3, lines 37-39).

Thus, Cox teach all the limitations of claims 4, 10, 16, 35, and 37, except for a memory controller bus coupled between a first and second memory controllers for passing memory access request from one memory controller to another memory controller.

However, as shown in Fig. 1, Ottinger teach a method and apparatus for processing memory requests, wherein as shown in Fig. 1, a computer system 10 comprises a first memory controller 24a coupled to a first memory 26a, and a second memory controller 24b coupled to the a second memory 26b, and an I/O bus 20 (memory controller bus) coupled between the two memory controllers. Ottinger also teaches the first MLST 28a (a first register) contains status information about each cached memory line of the first memory 26a (i.e. each memory line of the first memory 26a that is stored in the cache memories 36a-39a and 36b-39b). Likewise, the second MLST 28b (a second register) contains status information about each cached memory line of the second memory 26b. The first memory controller 24a utilizes the information stored in the first MLST 28a to determine whether a memory request on the first processor bus 30a requires a MIC request be issued to the second memory controller 24b via the I/O bus 20. Likewise, the second memory controller 24b utilizes the information stored in the second MLST 28b to determine whether a memory request on the second processor bus 30b requires a MIC request be issued to the first memory controller 24a via the I/O bus 20 (col. 7, lines 49-65).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Cox in combination with the method as taught by Ottinger in order to maintain coherency while processing memory requests (col. 2, lines 28-30).

In regard to claims 2, 9, 15, 17, 34, as shown in Fig. 2, Cox teaches each memory block (23, 25, 27, 29) comprising, for example, a 256 k-byte dynamic random access memory (DRAM) array (col. 4, lines 21-26), embedded in the memory modules 1-n.

Referring to claims 3, 5, 11, 18, 32-33, and 39, as cited above, Cox teaches undefined blocks or space may be left in the memory space if necessary, for example, to bypass a failed memory block (col. 5, lines 31-33). Cox further teaches the Memory Address Mask command (Opcode 40-4F) is utilized to assign the base address for the first memory module on the control link. The mask value corresponds to the upper 4 bits of actual addresses in a 16 megabyte memory system where a 1-megabyte block of memory equals 1 mask value. The mask command values range from 40 to 4F. The 0 to F hexadecimal values define the absolute starting block address in increments of 1 megabyte per block. If more than 1 megabyte of memory exists on a given memory module, the MCL controller 22 will sequentially build additional addressing for each additional block of 1 megabyte of memory (col. 10, lines 1-13). Thus, Opcode 40-4F is used to keep track of the number of functional sub-arrays in the memory module.

Referring to claims 6-7, and 12-13, 36, and 38, Cox teaches upon power up, the memory system controller automatically configures the memory system assigning an address to each of the memory module controllers in the network and a base address for the memory on each of the memory modules in the system (col. 2, lines 65-68, and col. 3, lines 1-2). Cox further teaches the

starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module. The process is repeated for each memory module 20 in turn until the entire memory space is defined. The starting addresses that are assigned to each of the individual memory modules 20 are referred to as base addresses. A specific memory module 20 will respond to addresses defined from [BASE] to [BASE+SIZE] (col. 5, lines 33-43).

4. Claims 20-25, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (U.S. Patent No. 6,160,562) in view of Cox (U.S. Patent No. 5,357,621) in view of Ottinger (U.S. Patent No. 6,070,231).

Referring to claims 22 and 28, as shown in Fig. 1, Chin et al. teach a computer system 10 comprising a CPU (system) bus coupled a system processor 12, a bus interface 14 coupled to the system bus, a graphics processor 20 coupled to the bus interface 14 through graphics bus AGP and also to memory (request) bus to access system memory 18, and a display 22 coupled to the graphics processor 20, which inherently includes a display logic to drive the display. Also included in the bus interface 14 is a memory controller 44 as shown in Fig. 2 and column 7, lines 24-26.

Thus, Chin et al. teach all the limitations of claims 22 and 28, except that the memory system comprising first and second memory arrays with faulty sub-arrays being left unassigned, and first and second memory controllers coupled to receive memory access requests, and a memory controller bus coupled between the first and second memory controllers to pass memory request from one memory controller to another.

However, as cited above, Cox teach a memory system comprising a plurality of memory modules, each of which includes a memory array, and a memory controller. As also cited above, Ottinger teach a method of transferring memory requests from one memory controller to another memory controller through a memory controller bus.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox and Ottinger incorporated into the computer system as taught by Chin et al. so as not to leave useable memory unallocated (Cox, col. 3, lines 37-39), and maintain coherency while processing memory requests (Ottinger, col. 2, lines 28-30).

In regard to claims 20, 27, and 29, although Chin et al. do not teach the first memory array comprising an embedded memory array, as cited above with reference to Fig. 2, Cox teaches each memory block (23, 25, 27, 29) comprising, for example, a 256 k-byte dynamic random access memory (DRAM) array (col. 4, lines 21-26), embedded in the memory modules 1-n.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox and Ottinger incorporated into the computer system as taught by Chin et al. so as not to leave useable memory unallocated (Cox, col. 3, lines 37-39), and maintain coherency while processing memory requests (Ottinger, col. 2, lines 28-30).

Referring to claims 21, 23, and 30, although Chin et al. do not teach the register storing a value indicative of the number of functional memory sub-arrays, Cox, as cited above, teach a register that keeps track of the functional memory arrays.

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox and Ottinger incorporated into the computer system as taught by Chin et

al. so as not to leave useable memory unallocated (Cox, col. 3, lines 37-39), and maintain coherency while processing memory requests (Ottinger, col. 2, lines 28-30).

Referring to claims 24-25, although Chin et al. do not teach storing a start and size defining the addressable memory area of the memory array, as cited above, Cox teaches the starting address of a newly added memory module 20 is calculated by adding the memory size of the preceding memory module to the starting address of that preceding memory module. The process is repeated for each memory module 20 in turn until the entire memory space is defined. A specific memory module 20 will respond to addresses defined from [BASE] (starting address) to [BASE+SIZE] (col. 5, lines 33-43).

Therefore, it would have been obvious to one skilled in the art to utilize the memory system as taught by Cox and Ottinger incorporated into the computer system as taught by Chin et al. so as not to leave useable memory unallocated (Cox, col. 3, lines 37-39), and maintain coherency while processing memory requests (Ottinger, col. 2, lines 28-30).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

H. Nguyen

11/18/2004